Syllabus

Course Title: VME Bus Architecture and Analysis

Date: Determined by Customer

Time: 6 hours

Location: Customer Facility

Instructor:

Paul Schur, President of Silicon Control Inc., has been developing computer hardware and software for the past 35 years. He graduated from the University of Illinois at Urbana with a Bachelors of Electrical Engineering degree in 1977. After graduation Paul worked at Northrop Defense Systems designing electronic countermeasures for the F-15, B-1 and other Air Force and Navy aircraft. In 1982 he joined Teradyne Telecommunications developing test equipment for telecommunication switching systems. After 7 years Paul left Teradyne to start Silicon Control designing and manufacturing computer diagnostic test equipment. Over the last 20 years at Silicon Control, Paul has developed advanced analysis tools for many different types of computer bus architectures. These tools include bus analyzers and testers for Multibus, VME, VXI, SCSI, PCI and PCI Express. In addition to product design at Silicon Control, Paul teaches classes in bus architecture and analysis.

Goals:

To obtain an in depth understanding of the VME Bus Specification and the operation of the VME850 Bus Analyzer.

Course Description:

This course presents a comprehensive examination of all aspects of the VME Bus specification and the capabilities and use of a VME analyzer. The following topics are covered:

1. VME Bus Overview – The specifications and elements that make up the VME bus along with a brief historical look of the development and enhancements to the bus over time.

2. Data Transfer Bus – The main VME bus that transfers data between devices. All aspects of the data transfer bus are covered including signals, protocols and timing.

3. Arbitration Bus – In systems where devices share a common bus, an arbitration scheme is required to control access. An arbiter grants access in response to requests to use the bus. Various priority schemes and operation are discussed.

4. Interrupt Bus – The bus that provides a mechanism to signal and service interrupts. The signals, operation and timing of interrupts and interrupt service routines are discussed.

5. Utility Bus – System functions such as clocks, reset and failure signals are discussed.

6. Electrical Specifications – The power supply and signal specifications for VME boards and backplanes are presented including signal levels, drivers and terminations.

7. Mechanical Specifications – Outlines and dimensions for various board and backplane types are presented.

8. Bus Enhancements – The VME bus has been enhanced to improve speed and performance with the addition of many new features to the original specification. VME64x, 2eVME and 2eSST are some of these new protocols. The VME instrumentation bus, VXI., is also presented.

9. New Specifications – Some of the newest serial bus architectures have been incorporated into VME such as PCI Express. The structure and protocols are radically different then the parallel architecture of the VME bus but share a common form factor.

10. VME Bus Analyzer – The features and operation of the VME850 bus analyzer to understand, diagnose and analyze system problems and performance of a VME bus is presented. Each analyzer feature is covered including state, waveform and performance analysis, exerciser and stimulus, anomaly detection and slave memory. The analyzer is controlled by either a windowed software interface or API software.

Course Outline:

1. VME Bus Overview
    a. Introduction
    b. Brief History
    c. Specifications
        i. Mechanical Specifications
        ii. Electrical Specifications
        iii. Functional Specifications
        iv. Nomenclature
    d. System Elements
        i. Master
        ii. Slave
        iii. Busses

1. Data Transfer Bus
2. Interrupt Bus
3. Arbitration Bus
4. Utility Bus

2. Data Transfer Bus
    a. Address
        i. Byte Locations
        ii. Byte Alignment
        iii. Data Strobes and LWORD
        iv. Address Modifiers
    b. Data
        i. Data Widths
        ii. Multiplexed
    c. Control Lines
    d. Transfers
        i. SCT
        ii. BLT
        iii. MBLT
    e. Operation
        i. Memory Write
        ii. Memory Read
        iii. Multiplexed
        iv. Read Modify Write
        v. Unaligned Transfers
        vi. Lock
    f. CR/CSR Registers
        i. Configuration ROM
        ii. Control and Status Register
    g. Timing
        i. Master
        ii. Slave
        iii. System
3. Arbitration Bus
    a. Functional Modules
    b. Priority Schemes
    c. Signals
    d. Operation
    e. Timing
4. Interrupt Bus
    a. Functional Modules
    b. Signals
    c. Operation
    d. Timing
5. Utility Bus
    a. System Clock
    b. AC Fail

   c. System Reset
   d. System Failure
   e. Serial Bus A
   f. Serial Bus B
6. Electrical Specifications
   a. Power Supplies
   b. Signal Levels
   c. Signal Drivers
   d. Signal Terminations
7. Mechanical Specifications
   a. Board
   b. Backplane
8. Bus Enhancements
   a. VME64x
   b. VXI
   c. 2eVME
   d. 2eSST
9. New Specifications
   a. VXS
   b. VPX
10. VME Bus Analyzer
   a. VME850 Analyzer Overview
      i. Introduction
      ii. Applications
      iii. Functional Overview
   b. State/Waveform Analysis
      i. Capture
      ii. Triggering
      iii. Filtering
   c. Performance Analysis
      i. Types of Analysis
         1. Bus Utilization
         2. Transfer Rate
         3. Latency
         4. Burst Distribution
         5. Statistics
      ii. Setup Parameters
   d. Exerciser
      i. Memory Transfers
      ii. Data Types
      iii. Block Transfers
      iv. Commands
   e. Stimulus
      i. Driving Bus Signals
      ii. Conditional Response
      iii. Applications

1. Pattern Generation
2. Simulate Hardware

iv. Pushing the Limits of the Bus

f. Slave Memory
   i. Slave Bus Memory
   ii. Programmable Address
   iii. Programmed Response
g. Protocol and Timing Violation
   i. Protocol Violations
   ii. Timing Violations
   iii. Capture Window Display and Trigger
h. Backplane Testing
   i. Signal Short
   ii. Power Short
i. AnalyzeIt Software
   i. Overview
   ii. Features
   iii. Main Windows
   iv. Demonstration
j. API Interface
   i. Overview
   ii. Environment
   iii. Communications
   iv. Operation
   v. Functions
k. Analyzer Applications
   i. Configurations
   ii. Examples

Suggested Reading Materials:

1. American National Standard for VME64 - ANSI/VITA 1-1994 (R2002)
2. American National Standard for VME64 Extensions - ANSI/VITA 1.1-1997 (R2003)