Syllabus

Course Title: PCI Bus Architecture and Analysis

Date: Determined by Customer

Time: 6 Hours

Location: Customer Facility

Instructor:

Paul Schur, President of Silicon Control Inc., has been developing computer hardware and software for the past 35 years. He graduated from the University of Illinois at Urbana with a Bachelors of Electrical Engineering degree in 1977. After graduation Paul worked at Northrop Defense Systems designing electronic countermeasures for the F-15, B-1 and other Air Force and Navy aircraft. In 1982 he joined Teradyne Telecommunications developing test equipment for telecommunication switching systems. After 7 years Paul left Teradyne to start Silicon Control designing and manufacturing computer diagnostic test equipment. Over the last 20 years at Silicon Control, Paul has developed advanced analysis tools for many different types of computer bus architectures. These tools include bus analyzers and testers for Multibus, VME, VXI, SCSI, PCI and PCI Express. In addition to product design at Silicon Control, Paul teaches classes in bus architecture and analysis.

Goals:

To obtain an in depth understanding of the PCI Bus Specification and the operation of the PMC850 Bus Analyzer.

Course Description:

This course presents a comprehensive examination of all aspects of the PCI Bus specification and the capabilities and use of a PMC analyzer. The following topics are covered:

1. PCI Bus Overview - The specifications and elements that make up the PCI bus along with a brief historical look of the development and enhancements to the bus over time.

2. Signals – The signals that comprise the PCI bus are defined. Signals can be grouped into address/data, control, arbitration, interrupt and system functions.

3. Operation – The transfer of data between devices is explained. The signals, protocols and timing involved in performing a transfer are presented in detail.

4. Configuration Space –Configuration space defines the identity, function and capabilities of a device on the bus as well as allowing the system to configure a device. The structure and definition of the configuration space is presented.

5. Electrical Specifications - The power supply and signal specifications for PCI boards and backplanes are presented including signal levels and timing.

6. Mechanical Specifications – Several PCI form factors are discussed including PCI, PMC and CompactPCI. Outlines and dimensions for various board and backplane types are presented.

7. New Specifications – The PCI bus has been enhanced to improve speed and performance with the addition of the 66 Mhz and PCI-X specifications. The new PCI Express specification is also presented.

8. PCI Bus Analyzer - The features and operation of the PMC850 bus analyzer to understand, diagnose and analyze system problems and performance of a PCI bus is presented. Each analyzer feature is covered including state, waveform and performance analysis, exerciser and stimulus, anomaly detection, compliance testing and target memory. The analyzer is controlled by either a windowed software interface or API software.

Course Outline:

1. PCI Bus Overview
    a. Introduction
    b. Brief History
    c. Features
    d. Specifications
        i. Mechanical Specifications
        ii. Electrical Specifications
        iii. Functional Specifications
        iv. Nomenclature
    e. System Elements
        i. Initiator
        ii. Target
2. Signals
    a. Address and Data
    b. Control
    c. Arbitration
    d. Interrupt
    e. System
    f. Error Reporting
    g. 64 bit Extension
    h. JTAG

3. Operation
    a. Commands
    b. Control
    c. Addressing
        i. Memory
        ii. I/O
        iii. Configuration
    d. Data Usage
    e. Transactions
        i. Read
        ii. Write
        iii. Terminations
    f. Arbitration
        i. Overview
        ii. Protocol
        iii. Latency
    g. Interrupts
    h. Error Reporting
        i. Parity
        ii. System
    i. 64 bit Extension
4. Configuration Space
    a. Overview
    b. Organization
    c. Functions
        i. Identification
        ii. Control
        iii. Status
        iv. Base Address Registers
5. Electrical Specifications
    a. Overview
    b. Signaling Levels
    c. AC Specifications
    d. DC Specifications
    e. Timing
    f. Pin Assignments
    g. Requirements
6. Mechanical Specifications
    a. PCI
    b. PMC
    c. CompactPCI
7. New Specifications
    a. 66 Mhz
    b. PCI-X
    c. PCI Express

8. PCI Bus Analyzer
    a. PCI850 Analyzer Overview
        i. Introduction
        ii. Applications
        iii. Functional Overview
    b. State/Waveform Analysis
        i. Capture
        ii. Triggering
        iii. Filtering
    c. Performance Analysis
        i. Types of Analysis
            1. Bus Utilization
            2. Transfer Rate
            3. Latency
            4. Burst Distribution
            5. Statistics
        ii. Setup Parameters
    d. Exerciser
        i. Memory Transfers
        ii. Data Types
        iii. Block Transfers
        iv. Commands
    e. Stimulus
        i. Driving Bus Signals
        ii. Conditional Response
        iii. Applications
            1. Pattern Generation
            2. Simulate Hardware
        iv. Pushing the Limits of the Bus
    f. Target Memory
        i. Target Bus Memory
        ii. Programmable Address
        iii. Programmed Response
    g. Protocol and Timing Violation
        i. Protocol Violations
        ii. Timing Violations
        iii. Capture Window Display and Trigger
    h. Compliance Testing
        i. PCISIG Checklist
        ii. Device Identification
        iii. Test Types
    i. Backplane Testing
        i. Signal Short
        ii. Power Short
    j. AnalyzeIt Software
        i. Overview

   ii. Features
   iii. Main Windows
   iv. Demonstration
k. API Interface
   i. Overview
   ii. Environment
   iii. Communications
   iv. Operation
   v. Functions
l. Analyzer Applications
   i. Configurations
   ii. Examples

Suggested Reading Materials:

1. PCI Local Bus Specification, revision 2.2 – PCISIG
2. IEEE Standard for a Common Mezzanine Card (CMC) Family - IEEE Std 1386-2001