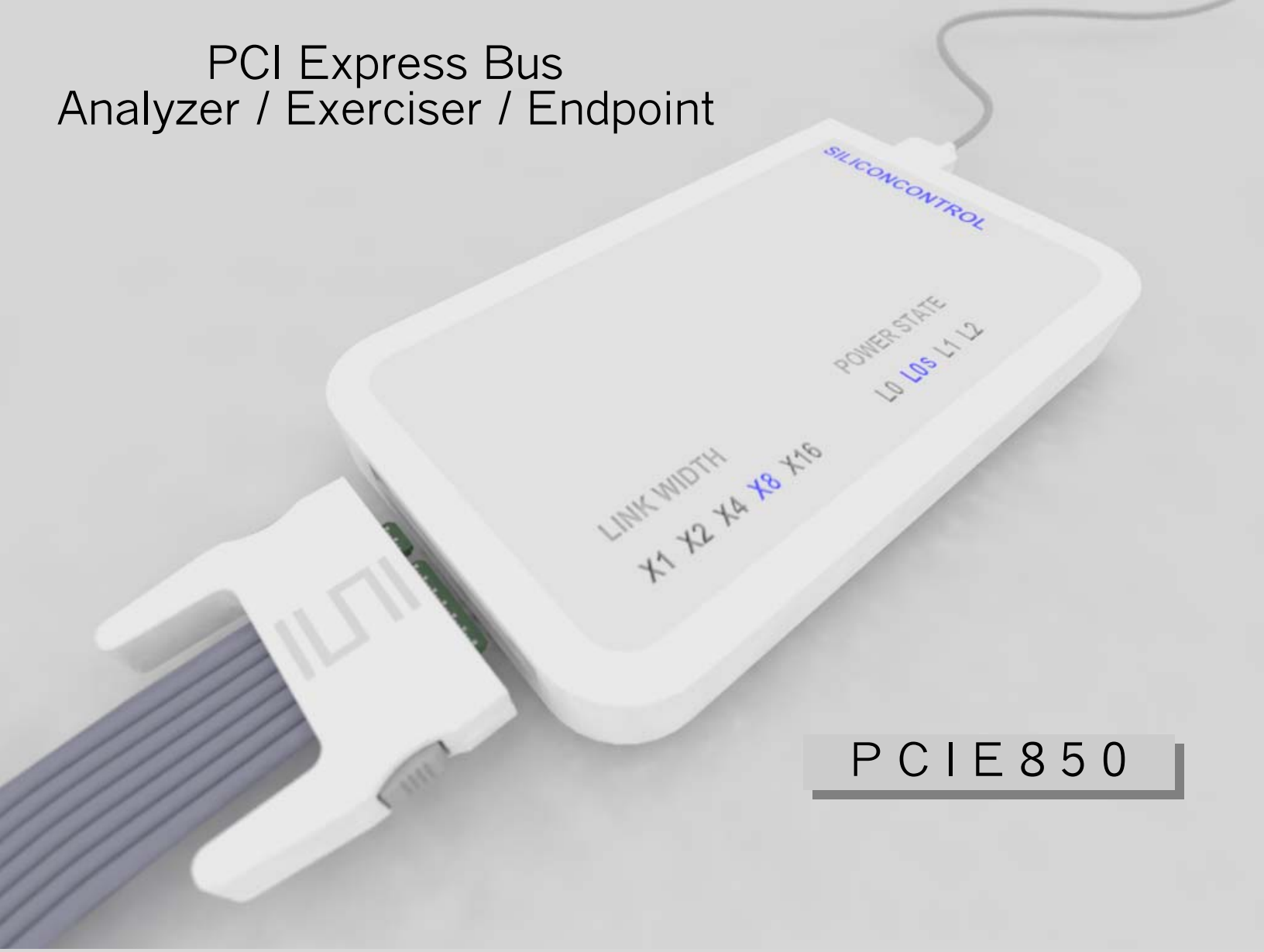
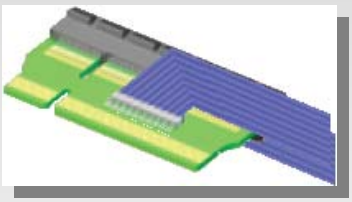
PCI Express Bus
Analyzer / Exerciser / Endpoint



PCIE850

Finally there is a powerful, flexible and affordable product for PCI Express bus analysis. The PCIE850 analyzes, exercises and emulates an endpoint to provide a complete test and debug solution. A wide variety of probes and interposers are available to match your application.

Interposer



Mid-Bus Probe

Flying Lead Probe

FEATURES

General

- x1, x4, x8, x16 Link Widths
- Dual x1, x4, x8 Link Analysis
- Link Speed 2.5 Gb/s
- Spread Spectrum Clock Support
- Passive Probes and Interposers
- USB and Ethernet User Interfaces
- AnalyzeIt and API Software

Analyzer

- Packet, Data and Lane Views
- Complex Triggers and Filters
- External Trigger Input/Output
- Statistical Analysis
- Protocol Error Checking
- Large Trace Memory
- Time Stamping

Exerciser/Endpoint

- TLP, DLP and PLP Generation
- Payload Data Generation
- Root Complex Emulation
- Link Training Control
- Error Injection
- Large Endpoint Memory
- Configuration Space

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PCIE850 SPECIFICATIONS

General Specifications

PCI Compliance:	PCI Express rev 1.1
Link Widths:	x1, x2, x4, x8, x16
Link Speed:	2.5 Gb/s
Clocks Supported:	On Board Precision Externally Supplied Spread Spectrum Clocking

Probes and Interposers

Probes:	Mid-bus spring contact PCB probe Flying Lead probe
Interposer Types:	Analyzer Exerciser / Analyzer Endpoint / Analyzer
Interposer Link Widths:	x1, x4, x8, x16

Analyzer Specifications

Trace Memory Size:	1GB
Sampling Rate:	2.5 Gb/s
Spread Spectrum Clock:	Supported
Link Widths Supported:	x1, x2, x4, x8, x16 Dual x1, x2, x4, x8
Capture Displays:	Packet View (TLP, DLP, PLP) Data View (Memory, I/O, Cfg) Lane View (Serial Bitstream)
Filters:	16 Conditions
Triggers:	16 Recognizers 8 External Triggers
Trigger Conditions:	Packet Header Fields Packet Data Payload Link Symbols Protocol Errors
Trigger Types:	Single Condition Logical Combination Sequential
Trigger Sequencer:	16 Levels If, Then, Else 16 Occurrence / Delay Counters 16 Filters 16 Event Conditions
Trigger Positions:	0%, 25%, 50%, 75%, 100%
External Inputs:	8 Front Panel Trace/Trigger
External Outputs:	1 Programmable Trigger Output
Time Tag Resolution:	4 ns
Time Tag Max Duration:	73 min.
Protocol Error Checking:	>50 anomalies
Statistics:	Event Counting Packet Types Payload Size

Exerciser Specifications

Clock Generation:	2.5 Gb/s
Spread Spectrum Clock:	Not Supported
Data Memory:	1MB
Physical Layer Support:	Symbol Generation Scrambling Lane Polarity, Reversal, Skew Link Widths x1, x4, x8. X16 Link Training
Data Layer Support:	DLLP Generation LCRC Generation Flow Control ACK/NAK Control
Transaction Support:	TLP Generation Payload Data Generation 2 virtual channels
Error Injection:	Physical Layer Errors Data Link Layer Errors Transaction Layer Errors

Endpoint Specifications

Endpoint Memory Size:	1MB
Spread Spectrum Clock:	Supported
Link Widths Supported:	x1, x2, x4, x8, x16
Payload Data:	Fixed Value Loaded File Patterns
Configuration Space:	Programmable
Error Injection:	Physical Layer Errors Data Link Layer Errors Transaction Layer Errors

Front Panel Interfaces

USB Port:	USB 2.0
Ethernet Port:	10/100 Mb/s
Probe/Interposer Port:	Differential 40 Channel
Indicators:	Link Width Link Power State Analyzer Power
External Power:	2 Conductor Circular
Trigger:	10 pin socket (8 in, 1 out, 1 ground)

Power Requirements Operating—5V at 3 Amps max
Standby—5V at 1 Amp max

Dimensions PCIE850—5”x 3” x 0.6”

Ordering Information

PCIE850	Analyzer / Exerciser / Endpoint
PCIEMBP	Mid-bus Probe
PCIEFLP	Flying Lead Probe
PCIEAn *	Analyzer Interposer
PCIEXn *	Analyzer/Exerciser Interposer
PCIENn *	Analyzer/Endpoint Interposer

* n = number of lanes