

The PCI650 - PCI Bus Analyzer / Exerciser

Analyzer

- Capture Bus Activity
- Event Recognition
- Complex Triggering and Filtering
- Time Stamping and Measurement
- State and Waveform Displays

Exerciser

- Memory, I/O, Config Transfers
- Generate Test Patterns
- Configuration Scanning
- Control Address / Data Width
- Read / Write to a File

Stimulus

- Fault Injection
- Control Bus Timing
- Hardware Simulation
- Pattern Generation
- Drive any Signal

Protocol Violation Checker

- Detects >50 Protocol Violations
- Master, Target and General
- Listed in State/Waveform Display
- Used as Trigger / Filter

Timing Violation Checker

- Checks Unstable Signals
- Setup and Hold Verification
- Glitch Detection

Performance Analysis

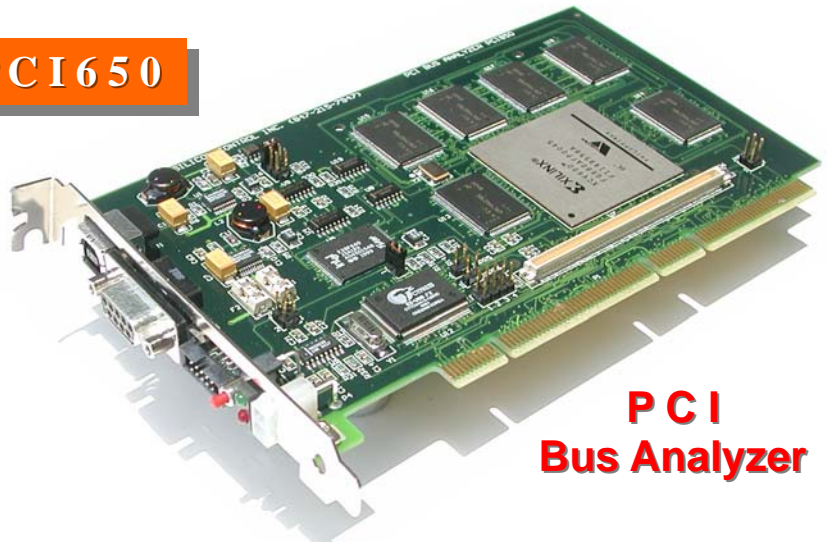
- Bus Utilization
- Transfer Rate
- Latency
- Burst Distribution
- Statistics

Windows and API Interface

- Analyzelt Windows Software
- User programmable API

Expansion Connector

PCI650



PCI
Bus Analyzer

The PCI650 Analyzer operates in 32 and 64 bit systems running from 0 to 66 Mhz. Over 100 protocol and timing violations are automatically checked and correlated with captured bus activity. System performance measurements include Bus Utilization, Transfer Rates, Latency, and Statistics.

Analyze It! Windows Software

CC	SAMPLE	COMMAND	ADDRESS32	DATA32	TIME[17:0]	DELTA	BUS DOCTOR
-3				33	40ns		
-2		I/O Wr	00000061	20	227ns		
-1					10ns		
0		I/O Rd	00000064	AE	94ns		
1				1C	53ns		
2		I/O Wr	00000064	AE	120ns		
3					94ns		
4		Int Ack	00000000	08	2.751us		
5					11ns		
6		I/O Rd	00000078	80	643ns		
7					53ns	60.25us	
8		I/O Wr	00000020	20	351ns		
9					10ns		
10		Int Ack	00000000	08	59.17us		
11					11ns		
12		I/O Rd	00000064	1D	981ns		
13					53ns		

Silicon Control introduces a lower cost analyzer and exerciser for PCI systems. The PCI650 offers many of the same features as our popular PCI850 bus analyzer without the Compliance Testing, Target Memory, PCI-X capability and Power Zoom. The result is a powerful diagnostic tool for bus analysis—all on a single plug-in card at an affordable price.



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THE LEADERS IN BUS ANALYSIS

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PCI650 SPECIFICATIONS

General Specifications

PCI Compliance:	PCI 2.2
Bus Size:	64 or 32 bit
Bus Signal Levels:	5V or 3.3V

Trace Specifications

Trace Memory:	
PCI650-1	128K by 144 bits
PCI650-2	256K by 144 bits
PCI650-3	512K by 144 bits
PCI650-4	1M by 144 bits
PCI650-5	2M by 144 bits
Sampling Rate:	66 Mhz
Sampling Modes:	System Clock System Clock w/ Address/Data System Clock w/ Transfers On board precision Oscillator (7.5ns to 15us)
Sampled Signals:	AD[63:0], C/BE[7:0], FRAME, DEVSEL, TRDY, IRDY, PAR, REQ, GNT, RST, LOCK, CLK, INTA, INTB, INTC, INTD, PAR64, PERR, SERR, REQ64, ACK64, TDO, TDI, TCK, TMS, TRST, SDONE, SBO, EXT[7:0]
External Inputs:	8 Front Panel Trace/Trigger
External Outputs:	1 Programmable Trigger Output
Triggers:	8 Trigger Conditions each Specifying 100 PCI Signals, 8 External Triggers and Anomaly
Trigger Types:	Single Condition Logical Combination 16 Level Sequencer
Trigger Positions:	0%, 25%, 50%, 75%, 100%
Occurrence Counters:	16 hardware counters 20 bits
Event Counters:	16 hardware counters 20 bits
Time Tag:	7.5 ns to 60 sec.

Exerciser Specifications

Initiator Bandwidth:	528 MB/s rate
Initiator Bus Width:	64 or 32 bit
Initiator Transfers:	Memory, I/O, Configuration

Front Panel Interfaces

RS232 Port:	DB9 connector, 110 to 115K Baud (cable included)
USB Port:	Series B connector, 12 MB/s (cable included)
Indicators:	GO LED, User LED
Pushbutton:	Reset Analyzer or System
External Power:	2 Conductor front panel (cable included)
Trigger:	10 pin socket (8 in, 1 out, 1 ground) (cable included)
Fuses:	Main power and External power

Power Requirements

Operating—5V at 3 Amps max
Standby—5V at 1 Amp max

Dimensions

PCI650—PCI Short Card

Ordering Information

PCI Analyzers

PCI650-1	PCI Bus Analyzer/Exerciser 128K Trace Buffer
PCI650-2	PCI Bus Analyzer/Exerciser 256K Trace Buffer
PCI650-3	PCI Bus Analyzer/Exerciser 512K Trace Buffer
PCI650-4	PCI Bus Analyzer/Exerciser 1M Trace Buffer
PCI650-5	PCI Bus Analyzer/Exerciser 2M Trace Buffer